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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,178	01/10/2002	Todd Edgar	MIO 0011 N2	3193

7590 11/21/2005

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,178	EDGAR, TODD	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 20 Oct. 2005 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5028990 to Kotaki et al. in view of US 5576240 to Radosevich et al.

Regarding claim 1, Kotaki discloses a storage container structure in fig. 10 comprising: a substrate 1, column 3 line 21, including a semiconductor structure; an insulating overlayer 6/8 disposed over and in contact with said substrate, insulating overlayer 6, column 4 line 25, including a container region 9 (groove), fig. 4b/9, disposed therein, said container region 9 defining a container cross section having

container side walls, a container bottom wall, and a container interior bounded in part by said container side walls and said container bottom wall; a patterning stop region 5b, column 3 line 23, fig. 10, disposed over said substrate 1 such that all of said container bottom wall is defined by an upper surface of said patterning stop region 5b, fig. 9; a charge storage lamina 12/13/14 over an interior surface of said container region 9; said charge storage lamina comprising a first conductive film 12, col. 3 line 29, a second conductive film 14, col. 3 line 31, defining a first surface thereon (junction between 14 and 16), and an insulating film 13, col. 3 line 30, disposed intermediate said first and second conductive films 12/14; a contact region (where 16 is located) defined by said charge storage lamina, wherein said contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein said contact region side walls and said contact region bottom wall are defined by said first surface of said second conductive film 14, fig. 10, and an electrical contact 16, column 4 line 68, in contact with said first surface of said second conductive film 14 such that said electrical contact 16 and said charge storage lamina 12/13/14 occupy collectively at least a portion of said container region.

But, Kotaki does not disclose a storage container structure such that a substantial entirely of the width of said container region is defined by an upper surface of said patterning stop region.

However, Radosevich disclose a storage container structure in fig. 1 comprises a lamina 14/15/17, col. 2 lines 58-63, a patterning stop region 12, col. 2 line 60, disposed over a substrate 11/18, col. 2 lines 61-62, such that a

substantial entirety of the width of said container region, fig. 2, is defined by an upper surface of said patterning stop region 12, fig. 1 or 2. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use storage container structure configuration teaching of Radosevich to replace Kotaki's storage container, because such configuration would have reduced the processing cost and had low voltage efficient of capacitance as taught by Radosevich in column 1 lines 55-60 and col. 2 lines 11-14.

Regarding claim 2, Kotaki discloses a storage container structure in fig. 10 comprising: a substrate 1 including a semiconductor structure; a patterning stop region 5B with a lower surface substantially coplanar with the top of said substrate1, fig. 10; an insulating overlayer 6 over said substrate, said insulating overlayer 6 comprising: a lower overlayer surface (bottom surface of 6) positioned over said substrate 1, wherein said lower overlayer surface is in contact with said top of said substrate 1, fig. 10, an upper overlayer surface (top surface of 6) and an intermediate overlayer 8 portion defined between said lower overlayer surface 6 and upper overlayer surface; a container region 9 within said insulating overlayer 6, container region 9 defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by container side walls and said container bottom wall, wherein all of container bottom wall is defined by an upper surface of said patterning stop region 5B, a charge storage lamina 12/13/14 over an interior surface of said container region 9; said charge storage lamina comprising a first conductive film 12, col. 3 line 29, a second conductive film 14, col. 3 line 31, defining a first surface

thereon (junction between 14 and 16), and an insulating film 13, col. 3 line 30, disposed intermediate said first and second conductive films 12/14; a contact region (where 16 is located) defined by said charge storage lamina, wherein said contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein said contact region side walls and said contact region bottom wall are defined by a first surface of said charge storage lamina 12/13/14, and an electrical contact 16 in contact with said first surface of said second conductive film 14 such that said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region, fig. 10.

But, Kotaki does not disclose a storage container structure such that a substantial entirely of the width of said container region is defined by an upper surface of said patterning stop region.

However, Radosevich disclose a storage container structure in fig. 1 comprises a lamina 14/15/17, col. 2 lines 58-63, a patterning stop region 12, col. 2 line 60, disposed over a substrate 11/18, col. 2 lines 61-62, such that a substantial entirety of the width of said container region, fig. 2, is defined by an upper surface of said patterning stop region 12, fig. 1 or 2. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use storage container structure configuration teaching of Radosevich to replace Kotaki's storage container, because such configuration would have reduced the processing cost and had low voltage efficient of capacitance as taught by Radosevich in column 1 lines 55-60 and col. 2 lines 11-14.

Regarding claim 3, Kotaki discloses a storage container structure comprising: a substrate 1 including a semiconductor structure, said substrate including a generally planar upper surface; an insulating overlayer 6 disposed over and in contact with said generally planar upper surface of said substrate 1, said insulating overlayer including a container region 9 disposed therein, said container region defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by container side walls and said container bottom wall; a patterning stop region 5B including: a lower surface substantially coplanar with generally planar upper surface of substrate 1; and an upper surface configured such that the lowermost extension of container bottom wall does not project substantially below upper surface of said patterning stop region 5B; a charge storage lamina 12/13/14 over an interior surface of said container region 9; said charge storage lamina comprising a first conductive film 12, col. 3 line 29, a second conductive film 14, col. 3 line 31, defining a first surface thereon (junction between 14 and 16), and an insulating film 13, col. 3 line 30, disposed intermediate said first and second conductive films 12/14; a contact region (where 16 is located) defined by said charge storage lamina, wherein contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein contact region side walls and contact region bottom wall are defined by a first surface of charge storage lamina 12/13/14; and an electrical contact 16 in contact region, wherein respective portions of electrical contact and charge storage lamina occupy collectively at least a portion of container region 9, fig. 10.

But, Kotaki does not disclose a storage container structure such that a substantial entirely of the width of said container region is defined by an upper surface of said patterning stop region.

However, Radosevich disclose a storage container structure in fig. 1 comprises a lamina 14/15/17, col. 2 lines 58-63, a patterning stop region 12, col. 2 line 60, disposed over a substrate 11/18, col. 2 lines 61-62, such that a substantial entirety of the width of said container region, fig. 2, is defined by an upper surface of said patterning stop region 12, fig. 1 or 2. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use storage container structure configuration teaching of Radosevich to replace Kotaki's storage container, because such configuration would have reduced the processing cost and had low voltage efficient of capacitance as taught by Radosevich in column 1 lines 55-60 and col. 2 lines 11-14.

Regarding claims 4-5, Kotaki discloses a storage container structure comprising: a substrate 1 including a semiconductor structure, substrate 1 including a generally planar upper surface, an insulating overlayer 6 disposed over and in contact with said generally planar upper surface of substrate, insulating overlayer 6 including a container region 9 disposed therein, container region defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by container side walls and said container bottom wall; a patterning stop region 5B including: a lower surface substantially coplanar with said generally planar upper surface of said substrate, fig. 10, and an upper surface substantially coplanar with said

container bottom wall; a charge storage lamina 12/13/14 over an interior surface of said container region 9; said charge storage lamina comprising a first conductive film 12, col. 3 line 29, a second conductive film 14, col. 3 line 31, defining a first surface thereon (junction between 14 and 16), and an insulating film 13, col. 3 line 30, disposed intermediate said first and second conductive films 12/14; a contact region defined by charge storage lamina, wherein contact region (where 16 is located) defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein contact region side walls and contact region bottom wall are defined by a first surface of charge storage lamina; and an electrical contact 16 in contact with said first surface of said second conductive film 14 such that said electrical contact 16 and said charge storage lamina 12/13/14 occupy collectively at least a portion of container region, fig. 10.

But, Kotaki does not disclose a storage container structure such that a substantial entirety of the width of said container region is defined by an upper surface of said patterning stop region or wherein said upper surface of patterning stop region 5B is configured such that all of container bottom wall is defined by said upper surface of said patterning stop region 5B, fig. 10..

However, Radosevich disclose a storage container structure in fig. 1 comprises a lamina 14/15/17, col. 2 lines 58-63, a patterning stop region 12, col. 2 line 60, disposed over a substrate 11/18, col. 2 lines 61-62, such that a substantial entirety of the width of said container region, fig. 2, is defined by an upper surface of said patterning stop region 12, fig. 1 or 2. At the time the

invention was made; it would have been obvious to one of ordinary skill in the art to use storage container structure configuration teaching of Radosevich to replace Kotaki's storage container, because such configuration would have reduced the processing cost and had low voltage efficient of capacitance as taught by Radosevich in column 1 lines 55-60 and col. 2 lines 11-14.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
Patent Examiner
10 Nov. 2005